CLAIMS

What is claimed is:

1. A method for evaluating a C++ description by an integrated circuit, comprising:

providing a C++ description including a C++ program;

storing said C++ program in a first memory module of an integrated circuit;

providing at least one of a scalar input and an input array to said integrated circuit;

executing said C++ program by a control device module of said integrated circuit; and

reading at least one of a scalar output and an output array from said integrated circuit.

2. The method of claim 1, further comprising:

storing each of said at least one of a scalar input and an input array, each of at least one of a scalar variable, a variable array, and a constant array, and each of said at least one of a scalar output and an output array into a separate memory module of said integrated circuit.

3. The method of claim 1, further comprising:

generating a first value at an output port of said integrated circuit by said control device module when said control device module executes said C++ program, said first value indicating said integrated circuit is busy; and

generating a second value at said output port of said integrated circuit by said control device module when said control device module finishes execution of said C++ program, said second value indicating said integrated circuit is available.

4. The method of claim 1, wherein said storing said C++ program step comprises:

translating said C++ program into a new program including low-level programming language commands; and

storing said new program into said first memory module.

5. The method of claim 4, wherein said low-level programming language commands are commands of Assembler programming language.

6. The method of claim 1, wherein said executing step is triggered when said control device module receives a value from an input port of said integrated circuit.

7. The method of claim 1, wherein said executing step comprising:

outputting an address by said control device module to said first memory module, wherein said address represents a command number;

outputting a command corresponding to said address by said first memory module to said control device module;

executing said command by said control device module; and

managing at least one of reading and writing of said at least one of a scalar input and an input array, at least one of a scalar variable, a variable array, and a constant array, and said at least one of a scalar output and an output array by said control device module.

8. The method of claim 7, further comprising:

calculating an address of a next command to be executed at a next clock cycle by said control device module.

9. An apparatus for evaluating a C++ description by an integrated circuit, comprising:

means for providing a C++ description including a C++ program;

means for storing said C++ program in a first memory module of an integrated circuit;

means for providing at least one of a scalar input and an input array to said integrated circuit;

means for executing said C++ program by a control device module of said integrated circuit; and

means for reading at least one of a scalar output and an output array from said integrated circuit.

10. The apparatus of claim 9, further comprising:

means for storing each of said at least one of a scalar input and an input array, each of at least one of a scalar variable, a variable array, and a constant array, and each of said at least one of a scalar output and an output array into a separate memory module of said integrated circuit.

11. The apparatus of claim 9, further comprising:

means for generating a first value at an output port of said integrated circuit by said control device module when said control device module executes said C++ program, said first value indicating said integrated circuit is busy; and

means for generating a second value at said output port of said integrated circuit by said control device module when said control device module finishes execution of said C++ program, said second value indicating said integrated circuit is available.

12. The apparatus of claim 9, wherein said means for storing said C++ program comprises:

means for translating said C++ program into a new program including low-level programming language commands; and

means for storing said new program into said first memory module.

13. The apparatus of claim 12, wherein said low-level programming language commands are commands of Assembler programming language.

14. The apparatus of claim 9, wherein said control device module starts execution of said C++ program when said control device module receives a value from an input port of said integrated circuit.

15. The apparatus of claim 9, wherein said means for executing comprising:

means for outputting an address by said control device module to said first memory module, wherein said address represents a command number;

means for outputting a command corresponding to said address by said first memory module to said control device module;

means for executing said command by said control device module; and

means for managing at least one of reading and writing of said at least one of a scalar input and an input array, at least one of a scalar variable, a variable array, and a constant array, and said at least one of a scalar output and an output array by said control device module.

16. The apparatus of claim 15, further comprising:

means for calculating an address of a next command to be executed at a next clock cycle by said control device module.

17. An integrated circuit for evaluating a C++ description including a C++ program, comprising:

a first memory module for storing a C++ program;

a plurality of memory modules, wherein each of at least one of a scalar input and an input array, each of at least one of a scalar variable, a variable array, and a constant array, and each of at least one of a scalar output and an output array are stored separately into each of said a plurality of memory modules; and

a control device module, communicatively coupled to said first memory module and said each of said a plurality of memory modules, for executing said C++ program and for managing at least one of reading and writing of said each of at least one of a scalar input and an input array, said each of at least one of a scalar variable, a variable array, and a constant array, and said each of at least one of a scalar output and an output array.

18. The integrated circuit of claim 17, wherein said first memory module is read-only memory.

19. The integrated circuit of claim 17, further comprising an output port communicatively coupled to said control device module, wherein said control device module generates a first value at said output port when said control device module executes said C++ program, said first value indicating said integrated circuit is busy, and wherein said control device module generates a second value at said output port when said control device module is not executing said C++ program, said second value indicating said integrated circuit is available.

20. The integrated circuit of claim 17, further comprising an input port communicatively coupled to said control device module, wherein a value at said input port starts execution of said C++ program by said control device module.